WHAT IS CLAIMED IS:

1. A method of performing a read operation from a memory cell in a memory cell string comprising:

applying a constant current across the memory cell string;

measuring a first voltage across the memory cell string;

writing the memory cell to a first state;

measuring a second voltage across the memory cell string; and

determining whether the first voltage differs from the second voltage.

2. The method of claim 1 further comprising:

determining that the memory cell was in a second state prior to being written to the first state in response to the first voltage differing from the second voltage.

3. The method of claim 2 further comprising:

reading out a logic level associated with the second state in response to the first voltage differing from the second voltage.

4. The method of claim 2 further comprising:

writing the memory cell to the second state in response to the first voltage differing from the second voltage.

5. The method of claim 1 further comprising:

determining that the memory cell was in the first state prior to being written to the first state in response to the first voltage not differing from the second voltage.

6. The method of claim 5 further comprising:

reading out a logic level associated with the first state in response to the first voltage not differing from the second voltage.

7. A data storage device comprising:

a memory cell string that includes a first memory cell and a second memory cell coupled in series;

a current source configured to apply a constant current across the string; and

a circuit coupled to the memory cell string, the circuit configured to detect a change in a voltage across the memory cell string in response to the current source applying the constant current across the memory cell string and the first memory cell being written to a first state.

8. The data storage device of claim 7 wherein the memory cell string has a first end and a second end, and wherein the current source is coupled to the first end.

9. The data storage device of claim 8 further comprising:

a ground source coupled to the second end of the memory cell string.

10. The data storage device of claim 7 wherein the circuit is configured to detect that the first memory cell was in a second state prior to being written to the first state in response to detecting a change in the voltage across the memory cell string.

11. The data storage device of claim 7 wherein the circuit is configured to detect that the first memory cell was in the first state prior to being written to the first state in response to not detecting a change in the voltage across the memory cell string.

12. A method of performing a read operation from a memory cell in a memory cell string comprising:

applying a constant voltage across the memory cell string;

measuring a first current across the memory cell string;

writing the memory cell to a first state;

measuring a second current across the memory cell string; and

determining whether the first current differs from the second current.

13. The method of claim 12 further comprising:

determining that the memory cell was in the first state prior to being written to the first state in response to the first current not differing from the second current.

14. The method of claim 13 further comprising:

reading out a logic level associated with the first state in response to the first current not differing from the second current.

15. The method of claim 12 further comprising:

determining that the memory cell was in a second state prior to being written to the first state in response to the first current differing from the second current.

16. The method of claim 15 further comprising:

reading out a logic level associated with the second state in response to the first current differing from the second current.

17. The method of claim 15 further comprising:

writing the memory cell to the second state in response to the first current differing from the second current.

18. A data storage device comprising:

a memory cell string that includes a first memory cell and a second memory cell coupled in parallel;

a voltage source configured to apply a constant voltage across the string; and

a means for detecting a change in a current across the memory cell string in response to the voltage source applying the constant voltage across the memory cell string and the first memory cell being written to a first state.

19. The data storage device of claim 18 wherein the first and second memory cells each have a first end and a second end, and wherein the voltage source is coupled to the first end of each of the first and second memory cells.

20. The data storage device of claim 19 further comprising:

a ground source coupled to the second end of each of the first and second memory cells.

21. The data storage device of claim 18 wherein the means is for detecting that the first memory cell was in a second state prior to being written to the first state in response to detecting a change in the current across the memory cell string.

22. The data storage device of claim 18 wherein the means is for detecting that the first memory cell was in the first state prior to being written to the first state in response to not detecting a change in the current across the memory cell string.